B1 Cont

leads formed on said frame body adjacent to said chip-receiving windows, and a plurality of external connection leads formed on said frame body adjacent to at least one of said chip-receiving windows; and

at least two integrated circuit chips, each of which is received in a respective one of said chip-receiving windows and has a plurality of bonding pads formed thereon, wherein said internal connection leads are electrically connected to said bonding pads on said integrated circuit chips in said chip-receiving windows to establish internal electrical connection among said integrated circuit chips, wherein said integrated circuit chip in at least one of said chip-receiving windows is a master integrated circuit chip, and said integrated circuit chip in other one of said chip-receiving windows is a slave integrated circuit chip, wherein said master integrated circuit chip includes an embedded testing circuit to permit testing of said slave integrated circuit chip that is connected thereto during a testing process of said semiconductor chip package; and

wherein said external connection leads are electrically connected to said bonding pads other than to bonding pads on said slave integrated circuit, said external connection leads serving as terminal pins such that external electrical connection with said integrated circuit chip in said at least one of said chip-receiving windows is established via said external connection leads.

10. The semiconductor chip package as claimed in Claim 9, wherein said internal connection leads are wire-bonded to said bonding pads on said integrated circuit chips in said chip-receiving windows.

11. The semiconductor chip package as claimed in Claim 9, wherein said external connection leads are wire-bonded to said bonding pads on said integrated circuit chips in said chip-receiving windows.

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12. The semiconductor chip package of Claim 9, wherein, during the testing process of said semiconductor chip package, said master integrated circuit chip is configured to receive stimulating signals via said external connection leads, to stimulate said slave integrated circuit chip via said internal connection leads in response to the stimulating signals, to receive stimulation response of said slave integrated circuit chip via said internal connection leads, and to output information corresponding to the stimulation response via said external connection leads.

REMARKS

Claims 9-12 are pending, with claims 1-8 being canceled herein.

The indicated allowability of claims 1-8 has been withdrawn in view of two new references, namely Yukio (JP 2-294061) and Taniguchi et al. (U.S. Pat. No. 6,134,161.)

The Examiner rejects canceled claims 1-6 under 35 U.S.C. 102(b) as being allegedly anticipated by Yukio.

Next, the Examiner rejects claim 7 under 35 U.S.C. 103(a) as being unpatentable over Yukio. The Examiner states that the prior art discloses all subject matter claimed but may not have classified the chips as master and slave IC's. Despite this, the Examiner states that there is nothing in the document that teaches away from that concept by limiting the application of the structure to specific integrated circuits and therefore it would have been obvious to one skilled in the art to consider the structure as applicable to such IC's since it is designed for all types of known IC's in the art.

Lastly, the Examiner rejects claim 8 under 35 U.S.C. 103(a) as being anticipated over Yukio in view of Taniguchi et al. The Examiner states that the prior art discloses all subject matter claim but omits an IC with embedded test circuits. However, the Examiner states that Taniguchi et al. teach the claimed elements in the Abstract and therefore it would have obvious to one skilled in the art to include